UDC 621.793.3:669.38

JIS

JAPANESE INDUSTRIAL STANDARD

Electroless copper platings

JIS H 8646-1991

Translated and Published

by

Japanese Standards Association

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Electroless copper platings — H 8646-1991

1. Scope

This Japanese Industrial Standard specifies the electroless copper plating (hereafter referred to as the "plating") 5 μm or thicker used for printed wiring boards by additive process.

Remarks 1. The printed wiring board by additive process used in this standard refers to a printed wiring board of which electroless copper plating method is applied to form conductor on a part or whole of surface of a base substrate.

2. The applicable standards to this Standard are listed below:

JIS B 7502-Micrometer Callipers for External Measurement

JIS B 7507-Vernier Callipers

JIS B 7721-Tensile Testing Machines

JIS C 5012-Test Methods For Printed Wiring Boards

JIS C 6480-General Rules of Copper-Clad Laminates for Printed Wiring Boards

JIS H 0400-Glossary of Terms Used in Electroplating

JIS H 0404-Graphical Symbol for Electroplated Coating

JIS H 1051-Methods for Determination of Copper in Copper and Copper Alloys

JIS H 8501-Methods of Thickness Test for Metallic Coatings

JIS K 1308-Nitric Acid

JIS K 1321-Sulfuric Acid

JIS P 8115-Testing Method for Folding Endurance of Paper and Paperboard by MIT Tester

JIS R 6253-Waterproof Abrasive Papers

JIS Z 8902-Xenon Standard White Light Source

Informative Reference: The additive process includes fully-additive process, semi-additive process, partial additive process, panel-additive process and pattern-additive process.

(1) Fully-additive Process A method of manufacture of circuits that through holes are based in an adhesive coated laminate, and wiring is formed only by electroless copper plating on the surfaces of flat portion and entire of holes.

(2) Semi-additive Process A method of manufacture of circuits that through holes are bored in an adhesive coated laminate, electroless copper plating is applied, and wiring is formed by electrolytic deposition and etching on the surfaces of flat portion and entire of holes.

(3) Partial-additive Process A method of manufacture of circuit that the wiring is formed on the flat surface by etching the copper foil of a copper-clad laminate, resist pattern for plating is provided thereon, and then only through-hole portions are coated by electroless copper plating.

(4) Panel-additive Process A method of manufacture of circuit that holes are bored in a copper-clad laminate, whole surfaces including through-thickness holes are coated by electroless copper plating, copper of unnecessary portions is removed by etching, and wiring is formed on the surfaces of flat portion and holes.

(5) Pattern-additive Process A method of manufacture of circuit that holes are bored in a copper-clad laminate, resist for coating is provided thereon, the wired portion on the flat surface and the through-thickness holes are coated by electroless copper plating, and copper of unnecessary portions on the flat surface is removed by etching.

2. Definitions of Terms

The definitions of principal terms used in this standard shall be as given in JIS H 0400.

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